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Multi-Domain System Support Environment for Multi-Core System

Renesas Technology Corp.
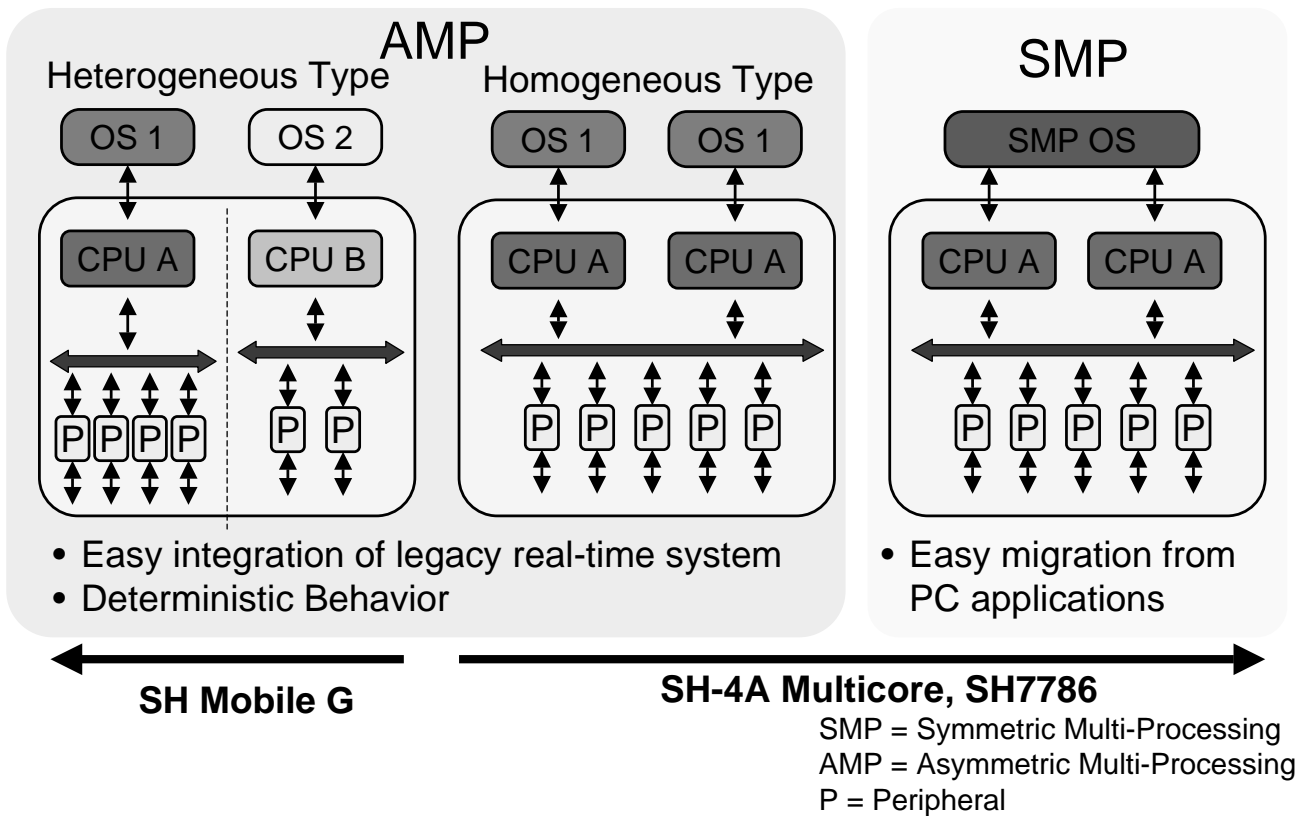
Toshihiro HATTORI

MPSoC 2008

June 26th, 2008
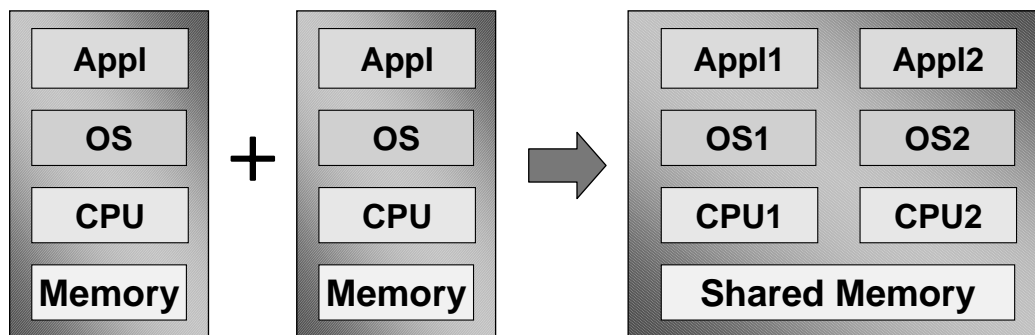

Agenda

- Multi-Core Chip as a Sub-system Integration
- Domain-base Multi-core Solution
    - Interoperation of Domains
        - EXREAL-ExARIA
    - Separation of Domains
        - EXREAL-ExVisor
- Demonstration
- Conclusions

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Multi-core Processor System OS Classes

AMP

Heterogeneous Type

OS 1   OS 2

CPU A   CPU B

P P P P   P P

Homogeneous Type

OS 1   OS 1

CPU A   CPU A

P P P P P

- Easy integration of legacy real-time system
- Deterministic Behavior

SH Mobile G

SMP

SMP OS

CPU A   CPU A

P P P P P

- Easy migration from PC applications

SH-4A Multicore, SH7786

SMP = Symmetric Multi-Processing
AMP = Asymmetric Multi-Processing
P = Peripheral

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AMP Configuration

- Design optimal system extension of embedded applications
  - To combine legacy systems
  - To guarantee real-time constrains (Deterministic behavior)

| Appl |
| OS |
| CPU |
| Memory |

+

| Appl |
| OS |
| CPU |
| Memory |

→

Appl1	Appl2
OS1	OS2
CPU1	CPU2
Shared Memory	

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Software Challenges of AMP

- Communication among OS:
  - Data transfer / Synchronization / Exclusion among tasks on multiple OS

- Future Portability
  - Software restructure is needed whenever HW configuration is changed

- Reliability
  - Shared HW resources (memory, IP, etc...) among multiple OS on a chip
  - Illegal access risk from different OS

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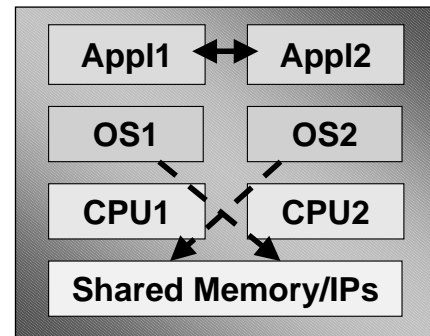
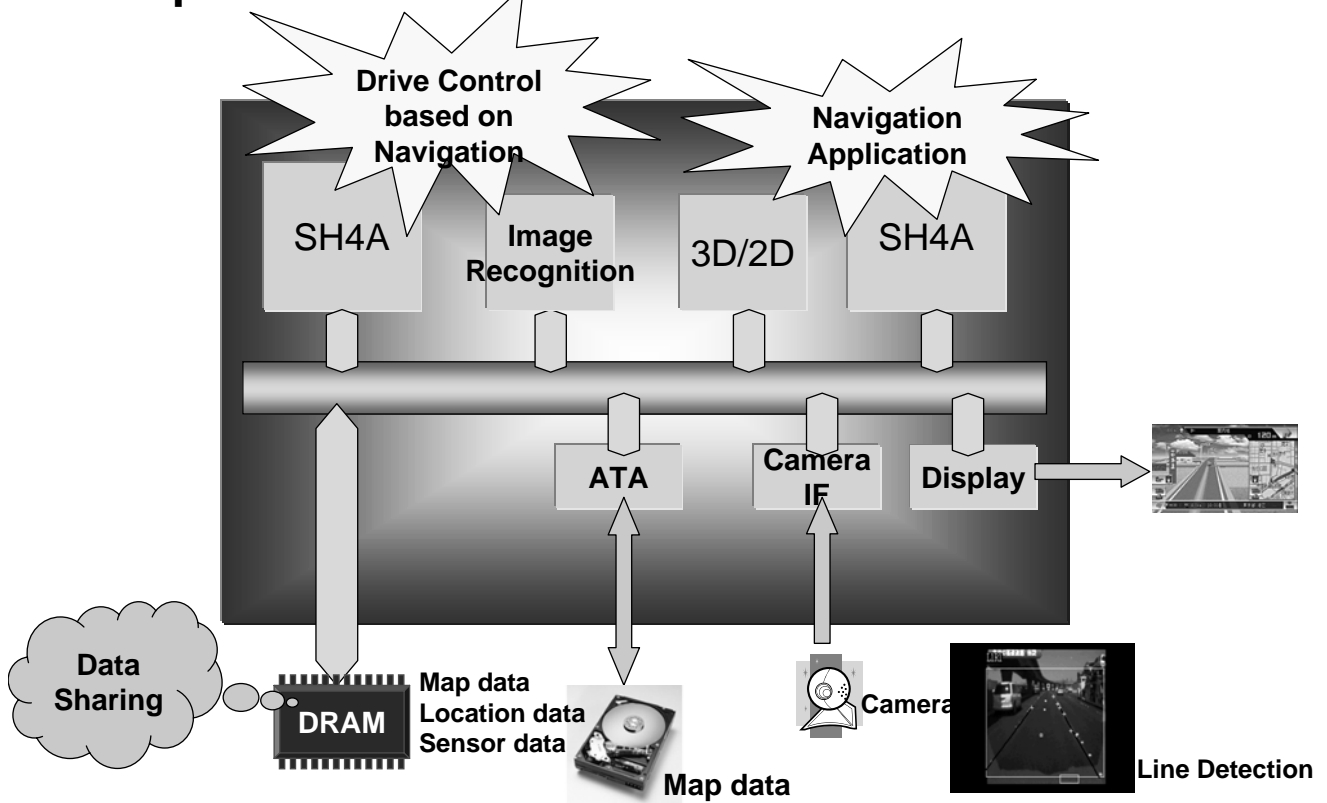
Interoperation / Separation Technology
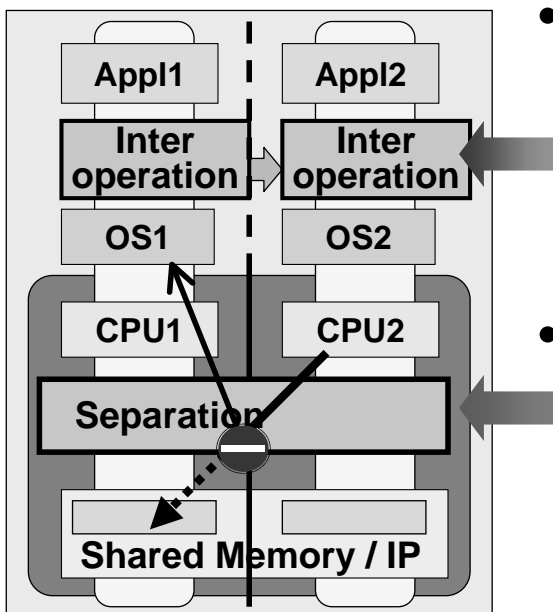
- **Interoperation** *EXREAL-ExARIA*
  - Communicate/ Synchronize among multiple heterogeneous OS
    - Common APIs like posix thread library
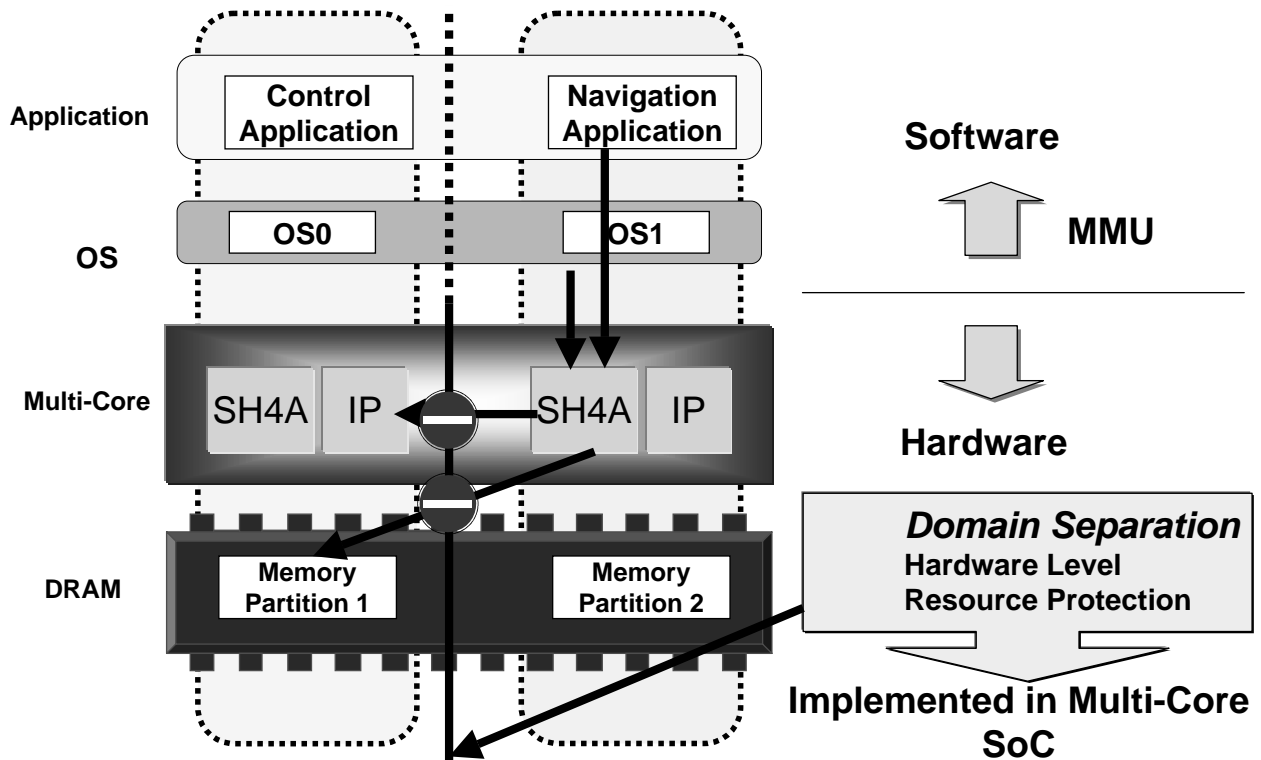 - Conceal HW configuration from SW designer

- **Separation** *EXREAL-ExVisor*
  - Isolate shared HW resources to a specific OS
  - protect / notify illegal access by HW support
    - Permission table of CPU ID and bus address
    - Illegal access interrupt to specified CPU

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Example of Target Application : Cooperation of Infotainment & Drive Control in Car

Drive Control based on Navigation

Navigation Application

SH4A

Image Recognition

3D/2D

SH4A

ATA

Camera IF

Display

Data Sharing

DRAM

Map data
Location data
Sensor data

Map data

Camera

Line Detection

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Domain Separation : Physical Memory Partitioning

Application

Control Application

Navigation Application

Software

OS

OS0

OS1

MMU

Multi-Core

SH4A

IP

SH4A

IP

Hardware

DRAM

Memory Partition 1

Memory Partition 2

Domain Separation
Hardware Level Resource Protection

Implemented in Multi-Core SoC

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HW/SW Structure of the Demonstration

- Heterogeneous OS AMP（WinCE **x** 2、uITRON **x** 2）

  - OS Domain Separation is using Hardware IP

  - Inter OS communication (Software Layer)

App reset	App graph	App idle prof	App Idle prof	App wireframe
inter-OS communication	inter-OS communication	inter-OS communication	inter-OS communication

"EXREAL-ExARIA"
Support Inter-OS Communication

uITRON	WCE	WCE	uITRON
access control	access control	access control	access control

"EXREAL-ExVisor"
Illegal Access Control with embedded hardware IP

SH-4A Multi-Core: CPU#0 | CPU#1 | CPU#2 | CPU#3

memory

Display U nit

serial | serial

Keypad

Access control of physical address space for each OS

Drive Control Domain | Infotainment Domain | Drive Control Domain

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Screen of the Demonstration

- Display Unit merges the frame buffer which each CPU(OS) draws
- CPU#0 Displays the CPU performance monitor which obtained by the inter-OS communication.

CPU#0 : uITRON 1	CPU#2 : Windows CE 5.0 (WCE 2)
CPU#1 : Windows CE 5.0 (WCE 1)	
	CPU#3 : uITRON 2

Summary

- Many approaches for multi-core solution exist.

- One of the realistic approaches for embedded system is sub-system integration.

- Domain (Software & Hardware) base design is proposed.

- Interoperation / Separation technologies help software development for AMP
  - Communication / Synchronization API among multiple OS
  - Resource protection from illegal accesses

- Demonstration:
  - WindowsCE® x 2 + uITRON® x 2
    with EXREAL-ExARIA and EXREAL-ExVisor

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